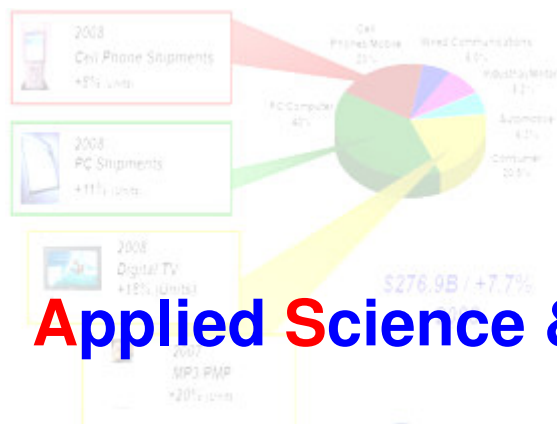


Flip Chip and Wafer-Level Chip Scale Packaging:

Market Updates, Key Processes and Application Examples



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Major References

- (33) Overview of ANST, 2008.
- (32) International WLP Conference, San Jose, CA, 2008.
- (31) Workshop on Flip Chip Technologies, Prismark, Hong Kong, 2008.
- (30) Advanced IC Packaging, Electronic Trend Publications, 2007.
- (29) Prismark Wireless Technologies Report, 2006, 2007, 2008.
- (28) KGD Conference, NAPA, CA 2004 and IWLPC, San Jose, CA, 2004.
- (27) APiA Seminar, Semicon-West, 2004.
- (26) Electronics Manufacturing with Lead-Free Materials, Lau, Wong, Lee & Lee, McGraw-Hill, 2003.
- (25) Area Array Interconnection Handbook, edited by Puttlitz and Totta, Kluwer Academic Publishers, 2001.
- (24) Low Cost Flip Chip Technologies, John Lau, McGraw-Hill, 2000.
- (23) The International Technology Roadmap for Semiconductors, 1999, 2000, 2001, 2002, 2008 Editions.
- (22) Chip Scale Package, Lau and Lee, McGraw-Hill, 1999.
- (21) Electronic Packaging: Design, Materials, Process, and Reliability, Lau, Wong, Prince, and Nakayama, McGraw-Hill, 1998.
- (20) Microelectronics Packaging Handbook, edited by Tummala, Rymaszewski, and Klopfenstein, second edition, Chapman & Hall, 1997.
- (19) Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies, Lau and Pao, McGraw-Hill, 1997.
- (18) Flip Chip Technologies, edited by J. Lau, McGraw-Hill, 1996.
- (17) Ball Grid Array Technology, edited by J. Lau, McGraw-Hill, 1995.
- (16) Chip on Board Technologies for Multichip Modules, edited by J. Lau, Van Nostrand Reinhold (VNR), 1994.
- (15) Handbook of Fine Pitch Surface Mount Technology, edited by J. Lau, VNR, 1994.
- (14) Multichip Module Technologies and Alternatives, edited by Doane and Franzon, VNR, 1993.
- (13) Surface Mount Technology - Recent Japanese Developments, edited by Jan Vardaman, IEEE Press, 1993.
- (12) Thin Film Multichip Modules, edited by Messner, Turlik, Balde, and Garrou, International Society for Hybrid Microelectronics, 1992.
- (11) Handbook of Tape Automated Bonding (TAB), edited by J. Lau, Van Nostrand Reinhold, 1992.
- (10) Solder Joint Reliability: Theory and Applications, edited by J. Lau, VNR, 1991.
- (9) Multichip Modules, edited by Johnson, Teng and Balde, IEEE Press, 1990.
- (8) Surface Mount Technology: Principles and Practice, Ray P. Prasad, VNR, 1989.
- (7) Microelectronics Packaging Handbook, edited by Tummala and Rymaszewski, VNR, 1989.
- (6) Electronic Materials Handbook, Volume 1, ASM International, 1989.
- (5) Principles of Electronic Packaging, edited by Seraphim, Lasky and Li, McGraw-Hill, 1989.
- (4) Proceedings of NEPCON West & East, SMI, ECTC, IEMT, IEPS, ICMCM, ISHM, and ITAP.
- (3) The National Technology Roadmaps by IPC, NEMI, and SIA.
- (2) IEEE Transactions on CPMT.
- (1) Magazines of EP&P, Surface Mount Technology, Advanced Packaging, and Circuits Assembly.

Outline

- **Executive Summary**
- **Flip Chip Packaging**
 - Market Updates
 - Key Processes
 - Application Examples
- **Wafer-Level Chip-Scale Packaging**
 - Market Updates
 - Key Processes
 - Application Examples
- **Summary**

Executive Summary

- This report studies the latest market trends & applications of flip chip (FC) and chip scale packages (CSP). Array package is going to be the main package format, where FC-CSP, wafer-level CSP, FC-BGA/PGA/LGA will have the highest growth rates.
- FC is more suitable for high I/Os (>300), high-end, high-performance –related applications, such as microprocessor, image processor, etc., whereas WLCSP is suitable for low I/Os (<28), low-cost applications such as integrated passives, analog/power devices, etc.
- Electroplating approach for under bump metallization and lead-free solder are going to be the main trends in flip chip package.
- The major challenges of WLCSP are: pitch reduction (350~400um), die size increment (upto 8x8mm²), increasing I/Os (>100), solder bump reliability and costs, etc.

Summary (1/3)

- **The market trend, key processes and application examples of flip chip package and wafer-level chip scale package have been reviewed.**
- **There are differences between FC and WLCSP (Please refer to the tables in following slides).**
- **The futures of FC would be primarily related to high pin counts, high performance applications while WLCSP would be more suitable for low pin counts, low-cost applications.**

Summary (2/3): WLCSP versus CSP versus Flip Chip

Features	WLCSP	CSP	Flip Chip
1. Packaging Level	One (Wafer Level Packaging)	One (Single Chip Packaging)	Zero (Chip Connection)
2. Types	OWRD, RDWE, OSRD, and WARD	Leadframe, Rigid or Flex Interposer	C4, FCOB/DCA, COG, PFC, E3, etc.
3. Normalized Footprint	1.0	< 1.5	1.0
4. Typical Bond Pitch	0.5 - 0.8 mm	0.5 - 1.0 mm	0.2 - 0.35 mm
5. Package Height	0.3 - 0.7 mm	LF: 0.5 - 1.4, IP: 0.8 - 2.0	0.5 - 0.7 mm
6. I/O Capability	< 200 (peripheral, full array or center depopulated)	400+ (peripheral, full array or center depopulated)	3000+ (full array or center depopulated)
7. Chip Connection	Wafer Processing	WB, TAB, or FC	Bumping (Evaporated, plated, printed, stud bump, etc.)
8. Design Issues	Escape routing, fan-in pitch, pad opening, etc.	Escape routing, fan-in vs. fan out, pad size, etc.	Escape routing, SMD vs. NSMD, die shrinking
9. Assy Issues	Solder volume, ball size/shape, mass reflow, etc.	Solder volume, pad size/shape, mass reflow	Solder volume, underfill, mass reflow etc.
10. Handling	Protected, standardizable (wafer, tray, t & r, tube)	Protected, standardizable (tray, tape and reel, tube)	Unprotected (wafer, tray, tape & reel or Gel-pak)

OWRD: On-Wafer/Chip Redistribution; RDWE: On-Wafer/Chip Redistribution with Encapsulation
OSRD: On-Substrate Redistribution; WARD: Wrap-Around & Redistribution

Summary (3/3): WLCSP versus CSP versus Flip Chip

Features	WLCSP	CSP	Flip Chip
11. Reworkability	O. K. for > 0.7 mm pitch	O. K. for > 0.7 mm pitch	O. K. for non-underfilled chips
12. Thermal	Challenging for devices with > 2 watts	Mainly for low power devices	Challenging for multichip configuration
13. Electrical	Good (key issues: signal/P/G distribution)	Good (key issues: signal/P/G distribution)	Excellent (key issues: alpha, particle, ESD, etc.)
14. Testability	Challenging	Improving, e.g. dual beam contact	Improving, e.g. KGD carrier technologies
15. Reliability (Package)	Bump voiding, uniformity, interfacial integrity, etc.	Popcorn, organic contamination, WB, underfill, etc.	Chip cracking, bump voiding, uniformity, etc.
16. Reliability (Board Assy)	Solder joint: pad size/shape, volume, surface finishing	Solder joint: pad size/shape, volume, surface finishing	Underfill volume, cracking, delamination, solder volume
17. Cost (pkg mat'ls + assy)	~\$100 to 200/wafer	LF: > TSOP, SOJ; IP: 0.8 - 3.5 cents/pin	<< \$100 to few \$100/wafer
18. Infrastructure	Matured	Matured (Japan is better than USA)	Matured
19. Key Enablers	Low cost redistribution, bumping, substrate, etc.	Low cost substrate, standardization, reflow, etc.	Low cost bumping, underfill, substrate
20. Key Applications	Memory, integrated passive, handheld, KGD, etc.	Handheld, memory, KGD	Microprocessor, ASIC, display driver, controller, etc.

~ **END** ~

Enquiry/comment/suggestion?

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